

REMARKS

Claims 1, 3, 5-12, 14-16, and 19-20 are pending in the application.

The Examiner allows claims 3, 6-12, 14-16, and 19-20. The Examiner allows claim 5 if rewritten to overcome an indefiniteness rejection under 35 U.S.C. § 112 and to include all of the limitations of the base and any intervening claims. The Examiner rejects claim 1 under 35 U.S.C. § 102(e) as being anticipated by Noji (U.S. Patent No. 6,138,255).

Applicants amend claims 1 and 5. Claims 1, 3, 5-12, 14-16, and 19-20 remain in the application.

Applicants traverse the claim rejections.

Applicants add no new matter and request reconsideration.

Claims Allowed

Applicants thank Examiner Nguyen for his allowance of claims 3, 6-12, 14-16, and 19-20.

Claims Allowable

Applicants amend claim 5 to obviate the Examiner's objection under § 112. Claim 5 is in condition for allowance.

Claim Rejections Under § 102(e)

Claim 1 recites *where during the test mode, the plurality of external signals have a voltage level higher than a power supply voltage*. The Examiner points to Noji's signal 10S as disclosing the recited *plurality of external signals*. Applicants point out claim 1 recites a *plurality of external signals*. That is, claim 1 recites two or more external signals, and not a single signal 10S as in Noji.

As explained in response to prior office actions, Noji's signal 10S varies within the confines of the power supply voltage, e.g., VCC. It does not disclose applying a voltage *higher* than a power supply voltage at any time, much less specifically during the test mode. Noji describes its system as follows: "In the normal operation mode, the voltage level of the reference signal 10S is set at an intermediate level (e.g., $\frac{1}{2}$ a power voltage VCC) between a 'LOW' level and a 'HIGH' level of the input signals ADR[0]-ADR[n]. In a test mode, the voltage level of the reference signals 10S is set at the same 'BELOW' level as that of the input signals." Noji, column 4, lines 22-28.

Noji does not explain what exactly is meant by the term BELOW but one can surmise that if the term "intermediate" is described as $\frac{1}{2}$ the power voltage VCC, then the term "BELOW" is likely less than $\frac{1}{2}$ the power voltage. That is, during the test mode, the signal 10S is less than $\frac{1}{2}$ the power voltage and not at a voltage level *higher* than the power supply level as recited. This interpretation is buttressed by an analysis of Noji's Figure 6.

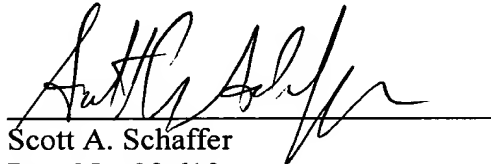
Conclusion

The Applicants request reconsideration and allowance of all claims as amended. The Applicants encourage the Examiner to call the undersigned if it appears an interview would be helpful in advancing the case.

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Respectfully submitted,

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